

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An imaging device, comprising:

a pixel array circuit that outputs an image signal and a background signal;

a memory array circuit, coupled to said pixel array circuit, said memory array circuit configurable to store an output from said pixel array; and

a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal.
2. The imaging device according to claim 1, wherein the imaging device further comprises an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.
3. The imaging device according to claim 2, wherein the imaging device further comprises an analog-to-digital converter,

which converts the signal received from the image enhancement circuit.

4. The imaging device according to claim 1, wherein each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit.

5. The imaging device according to claim 1, wherein an averaging circuit is coupled between the pixel array and the memory array to average pixel array outputs over multiple frames.

6. A method for processing analog image data in an imager chip, said method comprising the steps of:

receiving image data, said analog image data including a background signal and a temporal signal;

performing a subtraction operation to separate the background signal from the temporal signal; and

performing an enhancement operation on the temporal signal to generate an edge-enhanced signal.

7. The method according to claim 6, wherein the analog image data is received from a pixel array in said imager chip.

8. The method according to claim 6, wherein said analog image data is received from a memory array in said imager chip.

9. The method according to claim 6, wherein the background signal comprises an offset variation signal.

10. The method according to claim 6, wherein the background signal comprises a fixed pattern noise signal.

11. The method according to claim 6, further comprising the step of performing an analog-to-digital conversion to the edge-enhanced signal in said imager chip.

12. A pixel circuit, comprising:

a photodiode, coupled to a reset node;

a first transfer transistor, said first transfer transistor having a source terminal coupled to the reset node, a gate terminal coupled to a first transfer voltage line, and a drain terminal coupled to an output voltage node;

a pixel capacitor, coupled to said output voltage node; and

a second transfer transistor, said second transfer transistor having a source terminal coupled to said output voltage node, a gate terminal coupled to a second transfer voltage line, and a drain terminal coupled to an averaging capacitor.

13. The pixel circuit according to claim 12, wherein said reset node is coupled to a drain terminal of a reset transistor, said reset transistor having a gate terminal coupled to a reset voltage line, and a source terminal coupled to an operating voltage.

14. The pixel circuit according to claim 12, wherein said output voltage node is coupled to a gate terminal of a readout transistor, said readout transistor further having a source terminal coupled to the operating voltage, and a drain terminal coupled to a source terminal of a select transistor.

15. The pixel circuit according to claim 14, wherein said select transistor further has a gate terminal coupled to a select voltage line, and a drain terminal coupled to a pixel output line.

16. The pixel circuit according to claim 15, further comprising a data subtraction circuit, coupled to the pixel output line.

17. The pixel circuit according to claim 16, further comprises an edge enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

18. The pixel circuit according to claim 17, further comprising an analog-to-digital circuit that converts the signal received from the edge enhancement circuit.

19. The pixel circuit according to claim 18, further comprising a column address circuit, coupled to said analog-to-digital circuit, said column address circuit having a digital output line.

20. A method of operating a pixel circuit, said method comprising the steps of:

generating and storing a pixel voltage;

generating and storing a signal voltage;

reading out said pixel voltage via a source-follower circuit; and

filtering said stored pixel and signal voltage in an analog domain to produce a low-pass filtered pixel voltage output.

21. The method according to claim 20, wherein the step of filtering comprises passing the pixel voltage and signal voltage through a capacitive filter.

22. The method according to claim 21, wherein the low-pass filtered pixel voltage output may be expressed as:

$$\frac{C_A}{C_A + C_B} V_{pix(out)} + \frac{C_B}{C_A + C_B} V_{pix2}$$

wherein $V_{pix(out)}$ represents the pixel voltage, V_{pix2} represents the signal voltage, C_A represents a first capacitance associated with the pixel voltage in said capacitive filter, and C_B represents a second capacitance associated with the signal voltage in said capacitive filter.

23. The method according to claim 21, wherein a filter coefficient of said low-pass filtered pixel voltage output is C_B/C_A , wherein C_A represents a first capacitance associated with the pixel voltage in said capacitive filter, and C_B represents a second capacitance associated with the signal voltage in said capacitive filter.

24. The method according to claim 20, wherein the step of filtering further comprises subtracting the signal voltage from the pixel voltage.

25. An imager, comprising:

a row address circuit, said row address circuit having a plurality of control lines;

a pixel array, said pixel array comprising a plurality of pixel circuits, each of said plurality of pixel circuits being connected to said plurality of control lines and each pixel circuit having an output line;

a data subtraction array, said data subtraction array comprising a plurality of data subtraction circuits, each of said plurality of data subtraction circuits being coupled to a respective output line of said pixel circuit, and further being coupled to a first and second sample-and-hold line;

an edge enhancer array, said edge enhancer array comprising a plurality of edge-enhancement circuits, each of said edge enhancement circuits being coupled to a respective data subtraction circuit; and

an analog-to-digital converter array, said analog-to-digital converter array comprising a plurality of analog-to-digital converter circuits, each of said analog-to-digital converter circuits being coupled to a respective edge enhancement circuit.

26. The imager according to claim 25, wherein the control lines comprise a select line, a reset line, a first transfer line and a second transfer line.

27. The imager according to claim 25, wherein each pixel circuit comprises:

a photodiode, coupled to a resettable node;

a first transfer transistor, said first transfer transistor having a source terminal coupled to the resettable node, a gate terminal coupled to a first transfer voltage line, and a drain terminal coupled to an output voltage node;

a pixel capacitor, coupled to said output voltage node; and

a second transfer transistor, said second transfer transistor having a source terminal coupled to said output voltage node, a gate terminal coupled to a second transfer voltage line, and a drain terminal coupled to an averaging capacitor.

28. The imager of claim 25, wherein the data subtraction circuits comprise a first and second sample-and hold circuit, coupled respectively to the first and second sample-and-hold line, said first and

second sample-and-hold circuits being further coupled to a differential amplifier.

29. A method of operating an imager, said method comprising the steps of:

accumulating photo current in parallel in each of a plurality of pixel circuits in a pixel array;

sequentially selecting row lines in said pixel array;

sampling a first voltage in each row line after it becomes selected;

outputting said first voltage from said selected row line;

sampling a second voltage present in said selected row line after the first voltage is outputted; and

subtracting said second voltage from said first voltage to obtain an analog filtered data signal for each selected row line.

30. The method according to claim 29, said method further comprising the step of performing an edge enhancement operation on each analog filtered data signal from each selected row line.

31. The method according to claim 29, wherein the steps of sampling the first and second voltages comprises storing the voltage in a capacitive element.

32. The method according to claim 29, wherein the step of subtracting the second voltage from the first voltage comprises transmitting both voltages through a differential amplifier.

33. An imager, comprising:

a row address circuit, said row address circuit having a plurality of control lines;

a pixel array, said pixel array comprising a plurality of pixel circuits, each of said plurality of pixel circuits being connected to said plurality of control lines and each pixel circuit having a pixel output line;

a memory address circuit, said memory address circuit having a plurality of memory control lines;

a memory array, said memory array comprising a plurality of memory circuits, each of said plurality of memory circuits being connected to said plurality of memory control lines and to a respective

output line of a pixel circuit, each of said memory circuits having an memory output line;

a data subtraction array, said data subtraction array comprising a plurality of analog data subtraction circuits, each of said plurality of data subtraction circuits being coupled to a respective memory output line, and further being coupled to a first and second sample-and-hold line;

an edge enhancer array, said edge enhancer array comprising a plurality of analog edge-enhancement circuits, each of said edge enhancement circuits being coupled to a respective data subtraction circuit; and

an analog-to-digital converter array, said analog-to-digital converter array comprising a plurality of analog-to-digital converter circuits, each of said analog-to-digital converter circuits being coupled to a respective edge enhancement circuit.

34. The imager according to claim 33, wherein the control lines comprise a select line and a reset line.

35. The imager according to claim 33, wherein the memory control lines comprise a read line, a write line, and a transfer line.

36. The imager according to claim 33, wherein the memory circuits are further comprised of:

a first transistor, said first transistor being coupled to the pixel output line and to a voltage node;

a first capacitor, coupled between the voltage node and ground;

a second transistor, said second transistor being coupled to the voltage node and to a second capacitor, said second capacitor being further coupled to ground; and

a buffer amplifier, said buffer amplifier being coupled between the voltage node and a third transistor, said third transistor being further coupled to the memory output line.

37. The imager according to claim 36, wherein said first transistor has a gate terminal coupled to a write line, a source terminal coupled to the pixel output line, and a drain terminal coupled to the voltage node.

38. The imager according to claim 37, wherein said second transistor has a gate terminal coupled to said transfer line, a source terminal coupled to said voltage node, and a drain terminal coupled to said second capacitor.

39. The imager according to claim 38, wherein said third transistor has a gate terminal coupled to said read line, a source terminal coupled to said buffer amplifier, and a drain terminal coupled to the memory output line.

40. A method of operating an imager, said method comprising the steps of:

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storing a buffered pixel signal;

receiving a row output of a row in a pixel array;

storing the output

accumulating photo current in parallel in each of a plurality of pixel circuits in a pixel array;

sequentially selecting each of a plurality of row lines in
said pixel array;

storing a first analog voltage from a selected row line in
a memory circuit;

transmitting said first analog voltage from said memory
circuit to a data subtraction circuit;

receiving a second analog voltage from said selected row
line after the first voltage is outputted; and

combining said first and second analog voltage and
transmitting said combined voltage to a respective data
subtraction circuit in a data subtraction array, each of said data
subtraction circuit outputting a filtered data signal based on
the first and second analog voltages.

41. The method according to claim 40, said method further
comprising the step of performing an edge enhancement operation on
each filtered data signal from each selected row line.

42. The method according to claim 40, wherein the steps of storing said first and second analog voltages comprises storing the voltage in a capacitive element.

43. The method according to claim 40, wherein the data subtraction circuit comprises differential amplifier.

44. A circuit for filtering an image, comprising:

a first transistor, said first transistor being coupled to an output line of a pixel circuit and a voltage node;

a first capacitor, said capacitor coupled between the voltage node and ground;

a second transistor, said second transistor being coupled to the voltage node and to a second capacitor, said second capacitor being further coupled to ground; and

a buffer amplifier, said buffer amplifier being coupled between the voltage node and a third

transistor, said third transistor being further coupled to the memory output line.

45. The circuit according to claim 44, wherein said first transistor has a gate terminal coupled to a write line, a source terminal coupled to the pixel output line, and a drain terminal coupled to the voltage node.

46. The circuit according to claim 45, wherein said second transistor has a gate terminal coupled to said transfer line, a source terminal coupled to said voltage node, and a drain terminal coupled to said second capacitor.

47. The circuit according to claim 46, wherein said third transistor has a gate terminal coupled to said read line, a source terminal coupled to said buffer amplifier, and a drain terminal coupled to the memory output line.

48. An imager chip, comprising:

a substrate;

an array of pixel circuits formed in said substrate, each pixel circuit receiving light and, in response, providing a readout signal indicating light intensity;

processing circuitry, formed on substrate, said processing circuitry receiving readout signals from the array of pixel circuits and performing analog image processing on the readout signals; and

output circuitry, formed on the substrate, the output circuitry receiving processed readout signals from the processing circuitry, converting the processed readout signals to digital signals, and providing the digital signals as output from the imager chip.

49. The imager chip of claim 48, in which the processing circuitry performs at least one image processing operation from the set that includes background image subtraction and image enhancement.

50. A pixel circuit, comprising:

a light converting element that receives light and, in response, provides charge carriers;

a first capacitive element connected for receiving charge carriers from the light converting element, the first capacitive element storing a voltage indicating a quantity of charge carriers received;

a second capacitive element;

a switching element connected between the first and second capacitive elements and, when switched on, providing a conductive path through which a previous voltage stored by the second capacitive element is combined with the stored voltage from the first capacitive element; and

a readout element connected to provide a readout signal from the first capacitive element when the switching element is switched off and from the first and second capacitive elements when the switching element is switched on.

51. A memory circuit comprising:

an input lead for receiving a readout signal from a pixel circuit;

a first capacitive element connected to the input lead,
the first capacitive element storing a voltage indicating a level
of a received readout signal;

a second capacitive element;

a switching element connected between the first and
second capacitive elements and, when switched on, providing a
conductive path through which a previous voltage stored by
the second capacitive element is combined with the stored
voltage from the first capacitive element; and

a readout element connected to provide a readout signal
from the first capacitive element when the switching element is
switched off and from the first and second capacitive elements
when the switching element is switched on.

52. A processing system, comprising:

a memory unit;

a processing circuit coupled to said memory unit, said
processing circuit comprising:

a pixel array circuit that outputs an image signal and a background signal;

a memory array circuit, coupled to said pixel array circuit, said memory array circuit configurable to store an output from said pixel array; and

a data subtraction circuit, coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation on the pixel array output to remove said background signal from said image signal.

53. The processing system according to claim 52, wherein the processing system further comprises an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit..

54. The processing system according to claim 53, wherein the processing system further comprises an analog-to-digital converter, which converts the output signal from the image enhancement circuit.

55. The processing system according to claim 52, wherein each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit.

56. The processing system according to claim 52, wherein an averaging circuit is coupled between the pixel array and the memory array to average pixel array outputs over multiple frames.

57. An integrated circuit, comprising:

a substrate;

a pixel array circuit, formed in said substrate, for providing an image signal and a background signal;

a memory array circuit, formed in said substrate, coupled to said pixel array circuit for storing said image signal and background signal; and

a data subtraction circuit, formed in said substrate, coupled to said memory array circuit and said pixel array circuit, said data subtraction circuit performing a data subtraction operation to remove said background signal from said image signal.

58. The integrated circuit according to claim 57, wherein the integrated circuit further comprises an image enhancement circuit that performs an edge enhancement operation on the image signal received from the data subtraction circuit.

59. The integrated circuit according to claim 58, wherein the integrated circuit further comprises an analog-to-digital converter, which converts the signal output from the image enhancement circuit.

60. The integrated circuit according to claim 57, wherein each memory element in said memory array corresponds to a pixel circuit in said pixel array circuit.

61. The integrated circuit according to claim 57, wherein an averaging circuit is coupled between the pixel array and the memory array to average pixel array outputs over multiple frames.